512 bit Read/Write Multi-purpose Contactless Identification Device

Description

EM4205/4305 is a CMOS integrated circuit intended for use in electronic Read/Write RF transponders. It is suitable for low cost solutions like animal tagging applications. The IC communication protocol is compatible with the EM4469/4569 family.

The main difference between the EM4205 and EM4305 is that:

- EM4305 are bumped with enlarged pads for the two coil inputs. The enlarged bumped pads of the EM4305 transponder are intended for direct antenna connection avoiding the need of a module.
- EM4305 offers a 330pF resonant capacitor version

The IC is powered by picking up energy from a continuous 125 kHz magnetic field via an external coil, which together with the integrated capacitor form a resonant circuit. The IC reads out data from its internal EEPROM and sends it out by switching on and off a resistive load in parallel to the coil using a large modulation index. Commands and EEPROM data updates can be executed by 100% AM modulation of the 125 kHz magnetic field.

The EM4205/4305 supports bi-phase and Manchester data encodings.

The EM4205/4305 operating modes are stored in the EEPROM configuration word. All EEPROM words can be write-protected by setting protection bits.

The IC contains a factory programmed 32 bit unique identifier number (UID).

Features

- 512 bit EEPROM organized in 16 words of 32 bit
- 32 bit unique identifier (UID)
- 32 bit Password read and write protection
- ISO 11784 / 11785 Standard Compliant
- Lock feature converts EEPROM words into Read Only
- Two data encodings: Manchester and Bi-phase
- Multi-purpose data rate: 8, 16, 32, 40 and 64 RF clocks
- Reader Talk First feature
- Compatible with EM4469/EM4569 communication protocol
- 100 to 150 kHz frequency range
- On-chip rectifier and voltage limiter
- No external supply buffer capacitor needed
- -40°C to +85°C temperature range
- Very low power consumption
- Enlarged bumped pads (200 μm x 400 μm) for direct connection of coil (EM4305)
- EM4205: 2 resonant capacitor versions 210pF or 250pF selectable by mask option. The resonant capacitor can be trimmed, at factory level, to offer accuracy on the tolerance of 3%.
- EM4305: 3 resonant capacitor versions 210pF, 250pF or 330pF selectable by mask option
- Available in plastic extremely thin small outline package; 2 terminals; body 1.1 * 1.4 * 0.46 mm

Applications

- Animal Identification according to ISO FDX-B
- Pigeon races standard
- Waste management standard (BDE)
- Access Control
- Industrial

Typical Operating Configuration

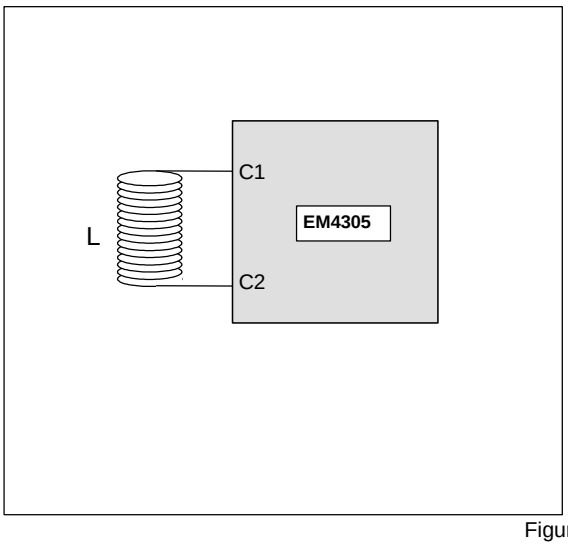

Figure 1

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Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Conditions
Input current on COIL1/COIL2	I_{COIL}	-30 to +30mA
Operating temperature range	T_{OP}	-40 to +85°C
Storage temperature range	T_{STORE}	-55 to +125°C
Electrostatic discharge to MIL-STD-883 method 3015 between Coil1 and Coil2	V_{ESD}	2000V

Table 1

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Care should be taken when the circuit is exposed to light. The circuit electrical parameters and functionality could vary with light intensity and are not guaranteed.

Handling Procedures

This device has built-in protection against high static voltages or electric fields. However, due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

Operating Conditions

V_{SS} = 0V

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_{OP}	-40	+25	+85	°C
AC voltage on coil pins	V_{COIL1}			(note)	V_{pp}
Maximum coil current	I_{COIL1}	-10		10	mA
Frequency on coil pins	F_{COIL1}	100	125	150	kHz

Table 2

Note: Maximum voltage is defined by forcing 10mA on Coil1 – Coil2

Electrical Characteristics

V_{REC} = 2.0 V, V_{SS} = 0 V, f_{COIL1} = 125 kHz square wave, V_{COIL1} = 4V_{PP}, T_{OP} = -40 to +85°C, unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Limiter voltage	V_{LIM}	I ($_{COIL2}$ - $_{COIL1}$) = ±10mA	7.7	8.4	9.1	V	
EEPROM write level seen from COIL1/COIL2	V_{WRC}		5			V_P	
Resonance capacitor	C_R	EM4205	202	210	218	pF	Note (1)
			240	250	260	pF	Note (1)
	C_R	EM4305	189	210	231	pF	Note (2)
			225	250	275	pF	Note (2)
			297	330	363	pF	Note (2-3)
EEPROM data retention	T_{RET}	T_{OP} = 55°C	10			years	Note (4)
EEPROM write cycles	N_{CY}	V_{DD} = 3.6 V	1000			cycles	

Table 3

Note 1: Resonant Capacitor trimming is only offered standard for the EM4205. In case that the trimming of the resonant capacitor is not done, tolerance range is the same as in EM4305.
Note 2: Statistics show a variation of capacitance within a wafer of ±3%
Note 3: The 330pF resonant capacitor version only available in EM4305
Note 4: Based on 1000 hours at 150°C.

Timing Characteristics

V_{DD} = 2.0 V, V_{SS} = 0 V, f_{COIL1} = 125kHz square wave, V_{COIL1} = 4V_{PP}, T_{OP} = 25°C,
Data rate f_{RF}/32, Bi-phase unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data Extractor timeout	t_{MONO}		20	40	60	µs
EEPROM programming time	t_{WEE}			9.34		ms
Protection words update time	t_{PR}			12.16		ms
Power check time	t_{PC}			1.48		ms
Power-up initialization	t_{PU}			3.3		ms
Processing Pause	t_{PP}			586		µs

Table 4

Data Extractor timeout (t_{MONO})

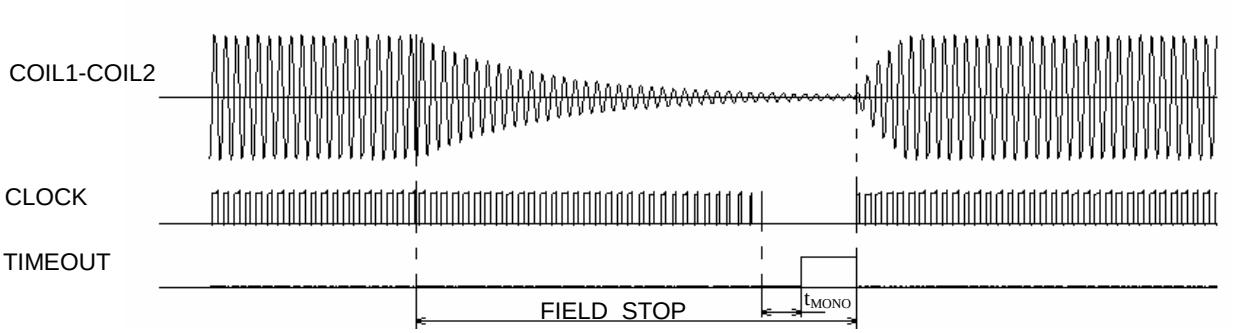


Figure 2

Transceiver field is amplitude modulated (field stops) to transmit data to the EM4205/4305. Data extractor detects absence of signal on coil terminals for period longer then T_{MONO}. Please note that the field has to be stopped for a much longer period of time than T_{MONO}. In figure above magnetic field is stopped when modulator switch is OFF. Second signal shows internal clock signal, which continues to be extracted up to the point where COIL1-COIL2 signal is lower then 1Vpp. Third signal, Timeout, indicates to the chip logic that a magnetic field stop was detected. The field stop detection time is at least T_{MONO} after the last extracted clock from the coil voltage. The length of transceiver field stop depends on the Q factor of the transponder. First field stop has to be longer (~18 - 20 RF cycles) since it is possible that it happens when chip modulator switch is off.

Power-up initialization (t_{PU})

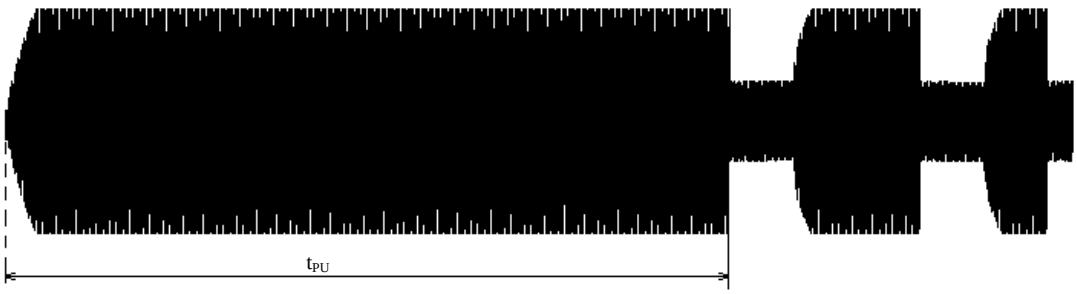


Figure 3

After the supply voltage crosses the POR threshold, the logic reads configuration word and then enters in default read mode. t_{PU} is the time from turning on transmitter field to start of the default read mode.

Block Diagram

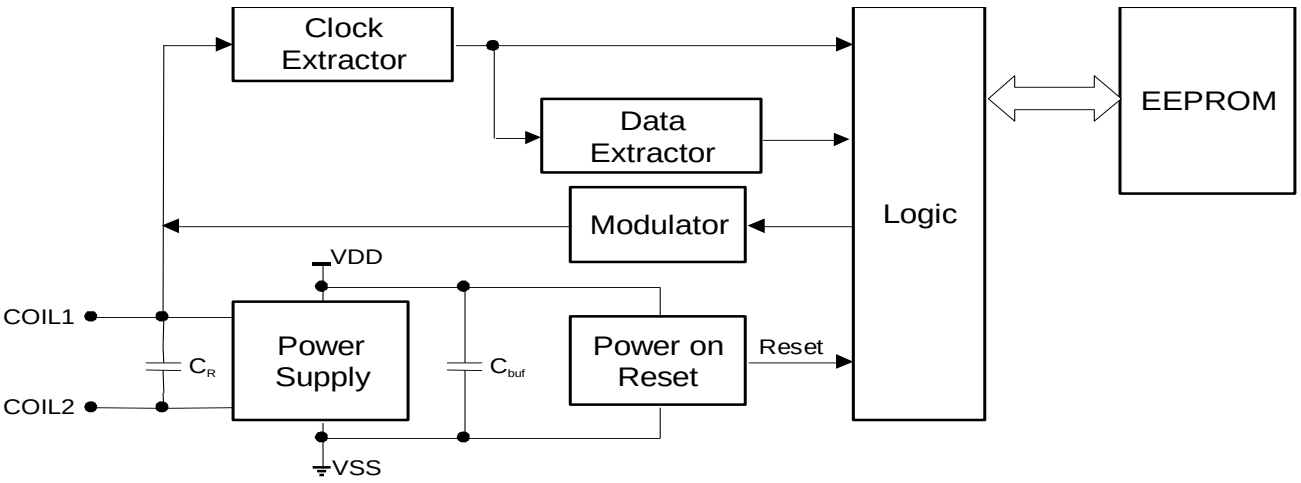


Figure 4

Functional Description

The IC builds its power supply through an integrated rectifier. When it is placed in a magnetic field the DC internal voltage starts to increase.

As long as the power supply is lower than the power on reset (POR) threshold, the circuit is in reset mode to prevent unreliable operation. In this mode, the modulator is switched off.

After the supply voltage crosses the POR threshold, the circuit reads configuration word and then enters in default read mode according to configuration just read. During the configuration word readout, the modulator switch is also off.

While the IC is operating in Default Read mode, it checks the coil signal to detect eventual command from reader. In the case the reader field stops for a period much longer than T_{MONO}, it interrupts read mode and expects reader to send the command. If a valid command pattern is detected then the command is executed. After execution of command the chip returns to default read mode.

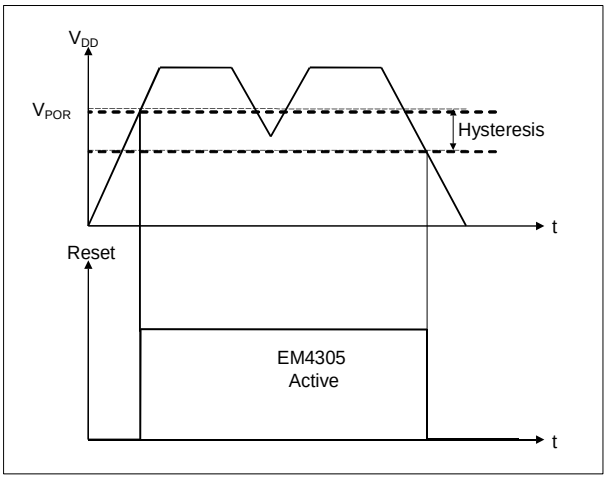


Figure 5

Block Description

Power Supply

This block integrates an AC/DC converter, which extracts the DC power from the incident RF field. It also acts as a limiter, which clamps the voltage on the coil terminals to avoid chip destruction in strong RF fields.

Power On Reset (POR)

When the EM4205/4305 with its attached coil enters the electromagnetic field, the built in AC/DC converter supplies voltage to the chip. The DC voltage is monitored and a Reset signal is generated to initialize the logic. The Power On Reset is also provided in order to make sure that the chip will start issuing correct data.
Hysteresis is provided to avoid improper operation at the limit level.

Clock Extractor

The Clock Extractor generates a system clock with a frequency corresponding to the frequency of the RF field (f_{RF}). The system clock is used by a sequencer to generate all internal timings.

Data Extractor

The transceiver generated field is amplitude modulated (field stops) to transmit data to the EM4205/4305. The Data Extractor detects absence of extracted clocks for periods longer than T_{MONO}.

Modulator

The Data Modulator is driven by Logic. When the Modulator is switched ON, it draws a large current from the coil terminals, thus amplitude modulating the RF field.

Logic

Logic is composed of several sub-blocks, which are described in the following text.

Controller
The Controller controls the state of the IC. Its main states are Power Off (power supply below POR level), Power-up Initialization, Default Read mode and Command processing.

Configuration Register
At power-up, when the power supply level gets higher than POR threshold, the content of the EEPROM Configuration word is transferred to the Configuration register to define default operating mode of the IC.

Sequencer
The Sequencer gets its clock signal from the Clock extractor and generates the Data Rate clock and other timing signals needed for operation of the other blocks. Data rate is defined by the number 'n' stored in the Configuration word.

Encoder

The Encoder encodes serial NRZ data before it is transmitted to the modulator switch. Two encoding options are implemented: Manchester and Bi-phase.

Command Decoder
The Command Decoder observes output of the Data Extractor. When a field stop is detected, it puts the Controller into Command Processing state and starts to decode the incoming data.

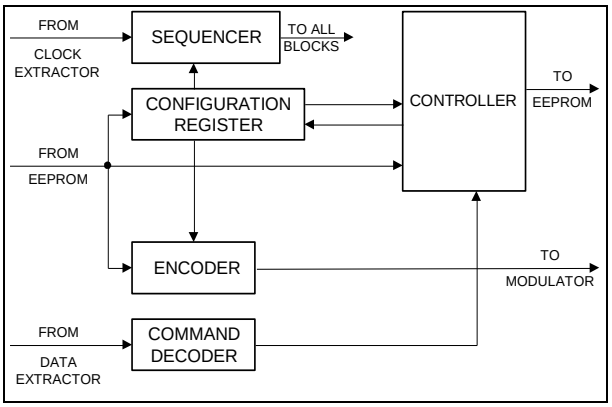


Figure 6

EEPROM Organization
512 bits of EEPROM are organized in 16 words of 32 bits.

The EEPROM words are numbered from 0 to 15.

The bits, in a word, are numbered from 0 to 31. The LSB first principle is always respected.

The 32 bits of EEPROM word are programmed with one Write Word Command.

Word 0 is assigned either to factory programmed Chip Type, resonant capacitor version and Customer Code number, or it can be reprogrammed by user to store some other data. Since this word is not part of the default message, it can be used to store some useful information which can only be accessed by the Read Word command.

Word 1 contains the IC unique identification number (UID) programmed at the factory. It can be accessed by a Read command.

Word 2 contains a 32 bit password. The password value can be changed only after a successful Login command.

Word 3 is a user free word. Similar to Word 0, it can store user specific information.

Word 4 is a Configuration word used to define the device-operating modes and options.

Words 5 to 13 are user free (288 bits) which can be part of a default message.

Words 14 and 15 are used to protect Words 0 to 13 from being modified using Write Word command.

Addr. (dec)	Description	Type	B_0,. ..,b_{31}
0	Chip Type, Res Cap Customer code/ User free	RW	ct_0 - Ct_{31}
1	UID number	RA	uid_0 - uid_{31}
2	Password	WO	ps_0 - ps_{31}
3	User free	RW	us_0 - us_{31}
4	Configuration word	RW	co_0 - co_{31}
5	User free	RW	us_0 - us_{31}
6	User free	RW	us_0 - us_{31}
7	User free	RW	us_0 - us_{31}
8	User free	RW	us_0 - us_{31}
9	User free	RW	us_0 - us_{31}
10	User free	RW	us_0 - us_{31}
11	User free	RW	us_0 - us_{31}
12	User free	RW	us_0 - us_{31}
13	User free	RW	us_0 - us_{31}
14	Protection word 1	RP	pr_0 - pr_{31}
15	Protection word 2	RP	pr_0 - pr_{31}

Table 5

Word types:
RA: access using Read Word command only
RW: access using Read Word and Write Word command
WO: access using Write Word command only
RP: access using Read Word and Protect command

Organization of Word 0

Word 0 is factory programmed with information on:
- Chip Type: fixed 4 bit number indicating member of the compatible family of chips.
- On-chip resonant capacitor values: 210pF, 250pF, or 330pF
- 10 bit Customer code

Word 0 can be reprogrammed by the user.

Chip Type
Bits ct_1 to ct_4 of Word 0 indicate the member of the compatible family of chips.

$Ct_1..ct_4$	**Chip Type**
1000	EM4205
1001	EM4305

Table 6

Resonant Capacitor
Bits ct_5 and ct_6 are used to indicate resonant capacitor value.

ct_5 - ct_6	**Resonant cap**
10	210 pF
01	250 pF
11	330 pF
other	not used

Table 7

Customer Code
Bits ct_9 to ct_{18} are attributed to Customer code. Default Customer code is 1000000000 (0x200 hex), where the leftmost bit is ct_{18}.
Bits ct_0, ct_7, ct_8 and ct_{19} - ct_{31} are reserved for future use and are set to 0.

Word 1: Unique Identification Number
Word 1 is factory programmed with 32 bit Unique Identification Number.

Word 2: Password Word
The 32 bit Password word has to be sent to the EM4205/4305 during a Login command to enable password protected operations.
The password word can not be read out with a read word command.

Word 4: Configuration Word
The Configuration word is used to define the device-operating modes and options, such as Encoder, Delayed On and Login Protection.

co_0 – co_5: Data Rate
Bits co_0 – co_5 define the data rate used by the EM4205/4305 to send back its data to the transceiver (in read only mode). The data rates are valid for both data encodings: bi-phase and Manchester.

Co_0 – Co_5	**Data Rate**
110000	RF/8
111000	RF/16
111100	RF/32
110010	RF/40
111110	RF/64
other	not used

Note 1

Table 8

Note 1: RF/40 data rate only available on the EM4305 – 330pF Cres version. RF/40 data rate is linked with Manchester and Biphase data encodings.

co_6 – co_9: Encoder
Bits co_6 – co_9 define the data encoding used by the EM4205/4305 to send back its data to the transceiver (in read only mode).

co_6 – co_9	**Encoder**
1000	Manchester
0100	Bi-phase
Other	not used

Table 9

co_{10}: Not used
This bit must be set to logic 0.

co_{11}: Not used
This bit must be set to logic 0.

co_{12} - co_{13}: Delayed ON
Bits Co_{12} - Co_{13} define the setting to allow control of the Delayed On feature. This mode follows the ISO 11785 specification to allow for time anticipation of low to high transitions. This feature is implemented for Bi-phase, and Manchester data encodings.

co_{12} – co_{13}	**Bi-phase Manchester**
00	No delay
01	Delayed On – BP/8
10	Delayed On – BP/4
11	No delay

Table 10

Since the Bit Period (BP) for Bi-phase and Manchester data encodings is selectable between RF/8, RF/16, RF/32 and RF/64, the Delayed On feature is defined relative to the bit period. The maximum Delayed On for Bi-phase and Manchester is one quarter of the bit period. Examples of Delayed On are shown in the figure below.

FDX-B mode: Bi-phase, RF/32
The example shown in the figure 8 is for the configuration as follows:
Delayed ON co_{12} – co_{13} = 10 => Delayed ON - BP/4

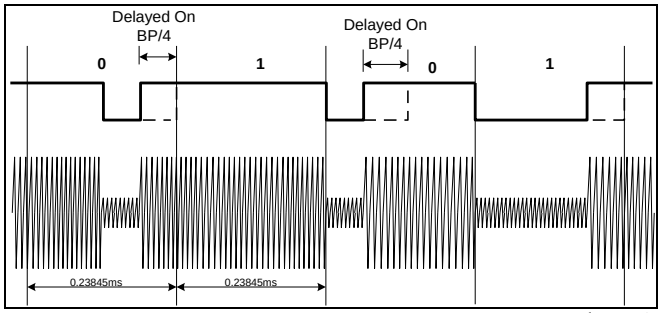


Figure 8

Note: For RF/40 data rate, the Delayed ON option is configured as following:

co_{12} – co_{13}	**Bi-phase Manchester**
00	No delay
01	Delayed On – 8 RF clocks
10	Delayed On – 16 RF clocks
11	No delay

co_{14}- co_{17} Last Default Read Word (LWR)
Bits co_{14} - co_{17} contain the binary word address of the last word read in default read. co_{17} is MSB and co_{14} is LSB. Please, note that the LWR valid range is from Word 5 up to Word 13.

co_{18}: Read Login
When set to logic 1, the reading of all words, except Words 0 and 1, by using the Read Word command is protected. Reading any of these words using the Read Word command, can be done upon successful execution of a Login command.

co_{19}: Not used
This bit must be set to logic 0.

co_{20}: Write Login
When the Write Login bit is set to logic 1, modification of EEPROM content is protected. Writing any word using Write Word command or changing protection using Protect command, can be done upon successful execution of a login command.
Note: Independent of write login configuration bit state, Password (word 2) reprogramming can be done upon successful execution of a login command.
.

co_{21} – co_{22}: Not used
These bits must be set to logic 0.

co_{23}: Disable
When this bit is set to logic 1, Disable command is accepted.

co_{24}: RTF (Reader Talk First)
When the RTF bit is set to logic 1, there is no modulation in Default Read mode, and the EM4205/4305 operates in Reader Talk First (RTF) mode. In RTF mode, the communication is done only using commands.

co_{25}: Not used
This bit must be set to logic 0.

co_{26}: Pigeon mode
When the Pigeon mode bit is set to logic 1, LWR definition (co_{14}- co_{17}) is ignored, EM4205/4305 starts to read the 32 bits of Word 5, then reads the 16 LSB bits of Word 6 and continue with the 16 LSB bits of Word 7.

After sending us_{15} of Word 7, readout continues without interruption with the first bit of Word 5.

This data structure permits the locking of48 bits of the pigeon code and allows modification of the last 16 bits before the race.

co_{27} - co_{31}: Reserved for future use
These bits must be set to logic 0.

Words 14 and 15: Protection Words

A mechanism is available to prevent individual EEPROM words from being modified by the write command. Memory locations 14 and 15 are used for this purpose (see table 5). They form a single Protection Register. Its content determines the write protection status of individual EEPROM words.

pr0 - pr13: Protection Bits
Bits pr0 to pr13 are used to write-protect individual EEPROM words, 0 to 13 respectively.

When set to 0, the corresponding EEPROM word can be modified through the Write Word command.

When set to 1, the word is write-protected and cannot be modified.

pr 14: Protection Bit
Bits pr14 is used to protect the Protection Register itself.

pr15: Status Bit
Bits pr15 is an internal status bit. Given the Protection Register implementation using two EEPROM words, pr15, when read as 1, identifies the currently active word. Currently active word holds the Protection Register content while the other non-active word is erased (all 0 content).

pr16 - 31: Not used
Bits pr16 - 31 are unused.

The Protection Register can only be modified through the Protect Command (see paragraph "Protect Command").

The Write Word command has no effect on the Protection Words.

The Read Word command can be used to read the Protection Words content.

Note: The above implementation, using two physical words in a read/write EEPROM to represent a single Protection Register, was chosen as an additional security feature. This double buffered mechanism caters to the fact an EEPROM-write operation internally generates an erase-to-zero operation followed by the actual write operation. Should the operation be interrupted for any reason (e.g. tag removal from the field) the double buffer scheme ensures that no unwanted "0"-Protection Bits (i.e unprotected words) are introduced.

EEPROM Delivery State

Default configuration is the following:

First two words (word 0 and 1) are programmed with:

- Chip Type
- Resonant capacitor version
- Customer Code
- Unique Identification Number (UID).

All the other user free memory words are set to 0.

The chip is initialized to Bi-phase data encoding, RF/32 clock data rate. Its LWR value is set to 8.

Default Read

After the supply voltage crosses the POR threshold, the circuit enters Power-up Initialization in which it reads the configuration word and then transitions to Default Read mode according to configuration just read.

In Default Read mode, the EM4205/4305 sends continuously its memory data starting from Word 5 and finishing with the last word according to the configuration word settings. After sending the last bit of the last word, readout continues without interruption with the first bit of Word 5.

Forward Link Communication
(Communication from the Reader to the Tag)

As already mentioned, the commands are sent from the reader to the tag by initiating a command while the EM4205/4305 is in default read mode. The communication is done by using 100% modulation index of reader field (also called field stops or OOK) with a bit timing of 32 periods of the RF field. The forward link communication protocol is identical to the EM4569/EM4469.

When the EM4205/4305 is in Default read mode, the logic permanently observes the Data Extractor output (see also Timing Characteristics and Block Diagram). The detection of field stop initializes the Command mode.

At reception of the first field stop, the IC stops immediately the default read and expects to receive a bit "0" to enter in the command processing mode. The transceiver and the chip are now synchronized and further data is sent. In the case where the first field stop is not followed by bit “0”, the IC returns in Default read mode.

The bit timing is composed of two states called MOD_ON and MOD_OFF (see figure 10). During the first 16 periods, the modulator is turned OFF (MOD_OFF) allowing the recharge of the internal supply capacitor. Then, the chip modulator is turned ON for the next 16 periods (MOD_ON). To receive a logic "0" bit, the IC has to detect a field stop before the end of MOD_ON state. If this field stop is not detected, a logic "1" is received.

Recommendations for Reader to Tag Timings

First Field Stop

It is recommended, but not required, that the reader sends the first field stop while the IC is in the MOD_ON state (modulator switch is ON). In that situation, the decay of the oscillations across the coil inputs is faster due to the low quality factor (modulator resistor brakes the Q factor). The reader has to stop the field for a long enough time to ensure oscillations on the tag coil terminals reduce from maximum possible amplitude to an amplitude below 800mVpp when the modulator switch is OFF and 100mVpp when modulator switch is ON. Additionally, the coil oscillations must remain below these thresholds for at least T_{MONO} time. Since the longest modulator OFF time in default read is 40 RF periods (FDX-B, data rate 32RF and delayed on BP/4), a first field stop of 55 RF clocks will be detected in all cases regardless of tag Q factor.

Sending a logic "1"

For sending a logic "1", the reader field shall stay ON for 32 RF periods.

Sending a logic "0"

When sending a logic "0", the reader field shall be stopped while the chip is in MOD_ON state.

In order to achieve reliable communication also for higher Q factors, it is proposed to send a logic "0" by keeping the reader field ON for 18 RF periods and switching it OFF for 14 RF periods. Increasing the field stops up to 23 RF periods improves communication robustness.

In first phase of 18 RF periods, the IC is at the end of MOD_OFF and starts MOD_ON. The reader field is OFF during a complete period with the IC modulator switch ON allowing maximum possible time to reduce amplitude of signal on tag coil (17 RF periods of 23 are used for this purpose). Additional 6 periods are here for the case that amplitude on coil was reduced below 0.8Vpp just at the end of MOD_ON state. In such a case, the field stop has to continue for a time longer than T_{MONO} to trigger the Data Extractor output.

Figure 10 presents an example of the reader to tag communication (read command of memory word 0) with the timings proposed above. Quality factor of tag coil is set to 30 and the field frequency is 125 kHz. First field stop is done during MOD_ON state (as recommended).

The digital signal represents the field modulation input of an electronic reader (i.e. EM4095 reader chip MOD pin). When this input is set to a high level, the field is switched OFF and when it is fixed to a low level, the reader chip generates a field.
The second signal corresponds to the signal across the EM4205/4305 coil inputs. The time base is 200us per square.

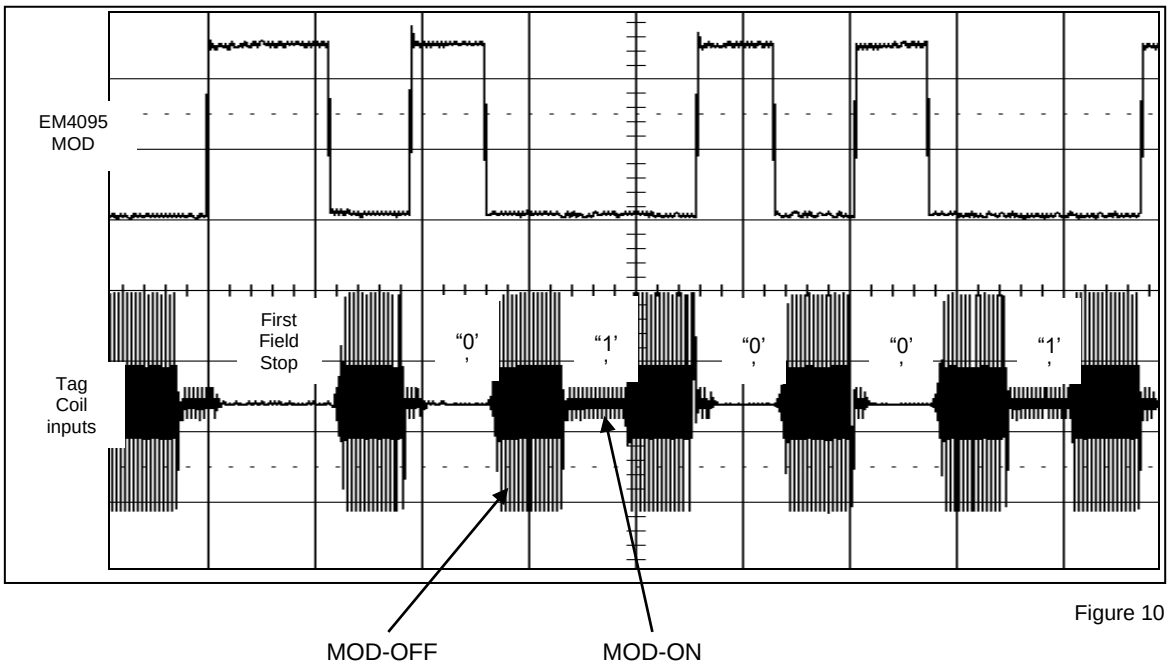


Figure 10

Commands

Command code structure:

All commands start by 3 bit command code, followed by command arguments. Possible command arguments are a word address and a 32 bit data field.

The 3 bit command code is terminated by an even parity bit:

cc_0	cc_1	cc_2	P

Table 11.a

Address structure:

The address field contains 4 bit address, two bits at 0 reserved for future use and an even parity bit.

A_0	A_1	A_2	A_3	"0"	"0"	P

Table 11.b

Data structure:

The 32 bit data field has an even parity bit inserted every 8 data bits, data is terminated with 8 column parity bits and a 0. Figure 11 represents the organization of command fields.

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	P_0
D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	P_1
D_{16}	D_{17}	D_{18}	D_{19}	D_{20}	D_{21}	D_{22}	D_{23}	P_2
D_{24}	D_{25}	D_{26}	D_{27}	D_{28}	D_{29}	D_{30}	D_{31}	P_3
PC_0	PC_1	PC_2	PC_3	PC_4	PC_5	PC_6	PC_7	"0"

Table 12

There are five commands implemented: Login, Write Word, Read Word, Protect and Disable.

$cc_0 – cc_2$	P	**Command**
001	1	Login
010	1	Write Word
100	1	Read Word
110	0	Protect
101	0	Disable

Figure 11

Upon successful decoding of first field stop followed by a logic "0" bit, the chip starts command decoding. In case command code is not corresponding to one of the four possibilities or parity bit is wrong command processing is interrupted and default read is resumed.

Login Command

Sending the Login command is necessary before sending any password protected command. In the Login command a 32 bit password including parity bits is sent as the command argument. The 32 bit password is sent according to the Data structure defined in table 12 (45 bits including parity). When the parity bits are correct and 32 bit password sent matches the content of Word 2, the login flag is set.

Login flag is set until the next power-up, which means that Login command has to be sent only once after power up to enable execution of password protected commands.

When the Login command is successfully processed, the IC responds with preamble pattern (00001010) and returns to Default Read mode.
When the Login is not accepted (wrong password or error in parity) error pattern 00000001 is sent and the IC returns to Default Read mode.

Write Word Command

In Write Word command the 4-bit word address is first sent followed by 32 bit data encoded according to the structure described in tables 11 and 12. During a write word sequence, it is recommended to place the EM4205/4305 in strong field conditions to ensure a correct EEPROM writing. In the case that the command is correctly processed, the EM4205/4305 checks whether the addressed word is not write protected or there is no parity error. It then checks if there is enough power available to program the EEPROM (Power check). In the case that all these conditions are fulfilled the EEPROM is written. After the EEPROM is written, the Configuration word is reloaded from the EEPROM, a preamble pattern (00001010) is sent and the chip returns to Default Read mode.

Loading of Configuration word is useful when the Configuration word has just been changed so that new settings are loaded.

If the Write Word command is not accepted (error in parity or at least one of the checks failed) error pattern 00000001 is sent and the IC returns to Default Read mode.

Read Word Command

In Read Word command the 4-bit word address is sent as command argument according to the structure described in table 11. When the command is correctly processed, a preamble pattern (00001010) followed by the content of the 32 bit word is sent. Please, note that the 32 bit data is sent using the command data structure

format (see table 12), which is not the same as in Default Read where only the data from the EEPROM is read.

When the Read Word command is not accepted (parity error), error pattern 00000001 is sent and the IC returns to Default Read mode.

Protect Command

The Protect command is used to protect EEPROM words 0 to 13 from being modified using Write Word command. In the Protect command, a 32 bit word is sent according to Data structure defined in table 12. Bits D_0 to D_{14} correspond to Protection bits pr_0 to pr_{14} (see Table 5). Bits D_{31} to D_{15} are don't care.

When the Protect command is successfully processed, the IC checks whether there is enough power available to program EEPROM (Power check) and updates Protection Words according to procedure which is described in paragraph "Words 14 and 15: Protection words". When this is finished preamble pattern 00001010 is sent and the chip returns to Default Read mode.

If the Protect command is not accepted (parity error or Power Check fail), Protection Words are not modified, error pattern 00000001 is sent and the IC returns to Default Read mode.

Disable Command

The Disable command is accepted when the Disable bit (co_{23}) of Configuration Word is set to 1.

In Disable command, an all-1 data field is sent as the command argument using the structure described in Table 12 (45 bits including parity bits, where parity bits are all 0). Command structure is therefore similar to Login command.

When this command is detected, the chip stops all operations until next power-up.

If the Disable command is not accepted (Disable bit set to 0, parity error or some other data then all-1), error pattern 00000001 is sent and the IC returns to Default Read mode.

Error during Command Detection

If a command code, which is not supported, or a command parity bit error is detected, the IC exits command processing and returns to Default Read mode without sending any message.

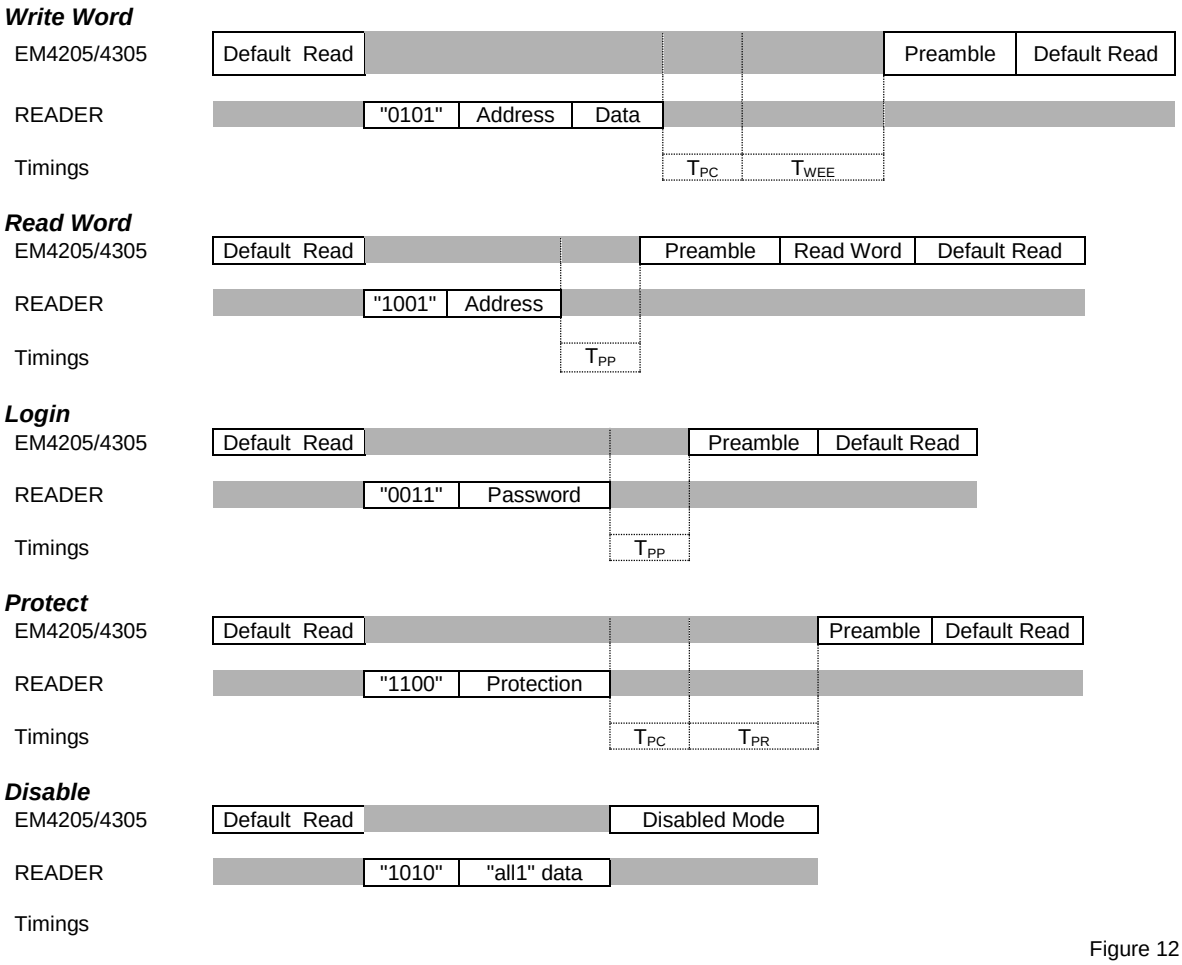


Figure 12

EM4205 – EM4305 state transition diagram

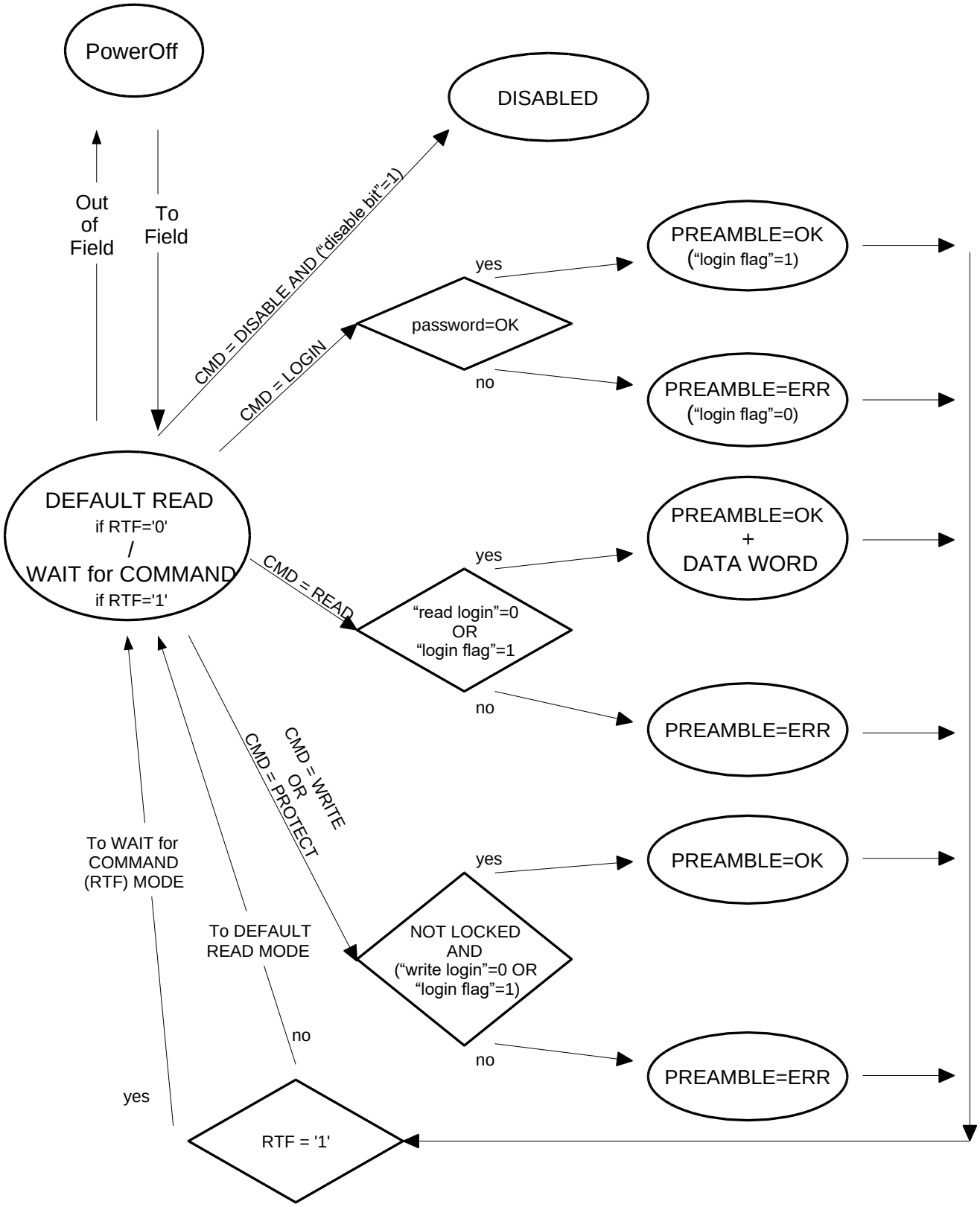


Figure 13

Return Link Encoder

(Communication from Tag to Reader)
In read mode, the NRZ data coming from the EEPROM flows (Default read or answer to Read Word command) through the Encoder before it is transferred to the Modulator. A logic 1 (high) means the Modulator is on.

Manchester

In Manchester coding, there is a transition from High to Low or from Low to High in the middle of the bit period. When a logic 0 is transmitted, the output is Low during the first half of the bit period and is High during the second half of the bit period. When a logic 1 is transmitted, the output is High during the first half of the bit period and is Low during the second half of the bit period.

Bi-phase:
In Bi-phase coding, there is a transition from High to Low or from Low to High at the beginning of each bit period. When a logic 0 is transmitted there is an additional transition in the middle of the bit period. When a logic 1 is transmitted there is no transition in the middle of bit period.

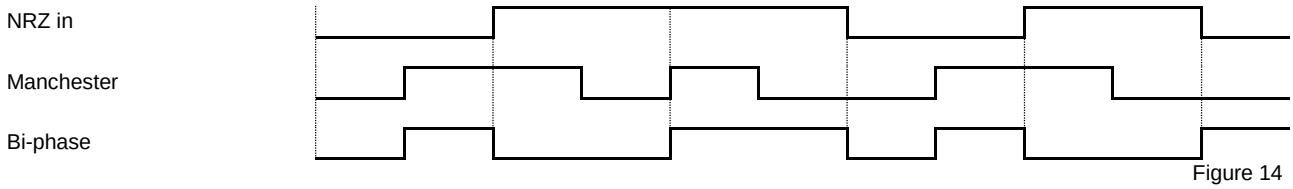


Figure 14

Examples of possible configurations

Pigeon Races: Manchester – RF/64 mode
In pigeon races, the EM4205/4305 uses a Manchester data encoding. The duration of a data bit corresponds to 64 periods of the magnetic field (data rate of RF/64).
Pigeon configuration bit (Co_{25}) has to be set to logic 1.

The pigeon code is programmed in Words 5, 6 and 7. The EM4205/4305 starts to read the 32 bits of Word 5, then reads the 16 LSB bits of Word 6 and continues with the 16 LSB bits of Word 7.

The pigeon code has to be programmed as following:
- Word 5: 32 first bits which corresponds to bit 0 up to bit 31 of the pigeon code
- Word 6: 16 LSB bits which corresponds to bit 32 up to bit 47 of the pigeon code
- Word 7: 16 LSB bits which corresponds to bit 48 up to bit 63 of the pigeon code

This data structure permits to lock 48 bits of the pigeon code and allows the modification of 16 bits before the race.

FDX-B: Livestock Applications
In FDX-B mode, the EM4205/4305 sends back to the reader, its memory contents from word 5 up to word 8 (128 bits) using a bi-phase data encoding and a data rate of RF/32. The duration of one bit is 32 magnetic field periods.

EM4205 Pad Location

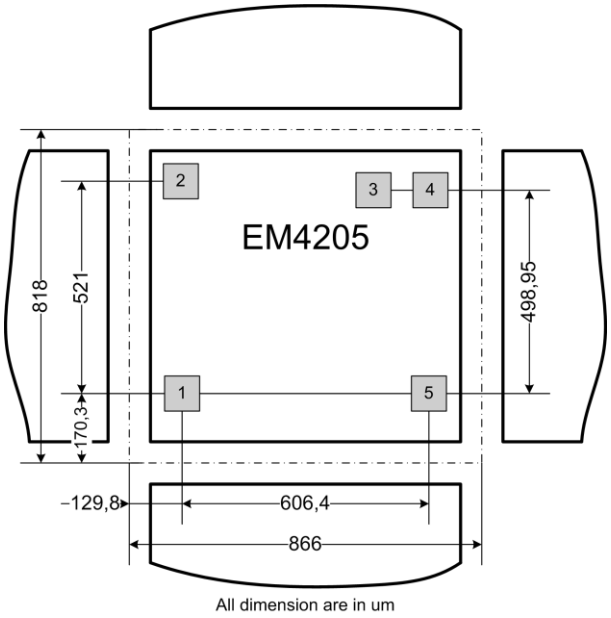


Figure 15

EM4305 Pad Location (V1, V2 and V3)

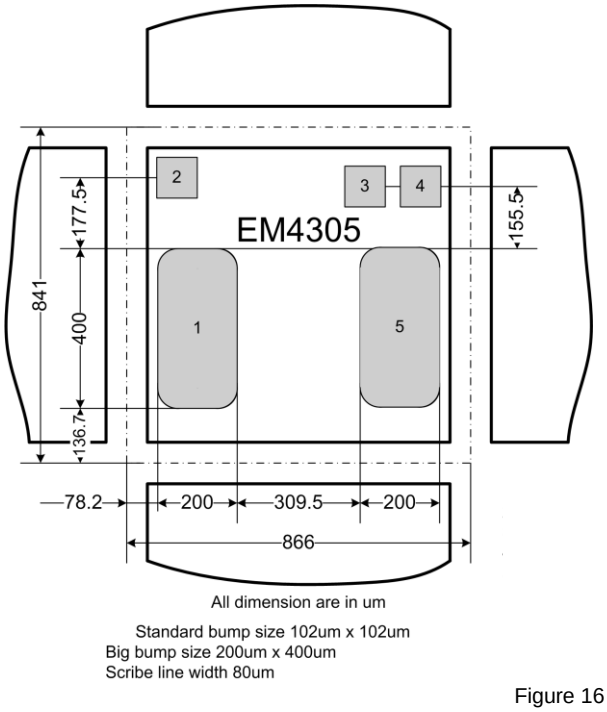
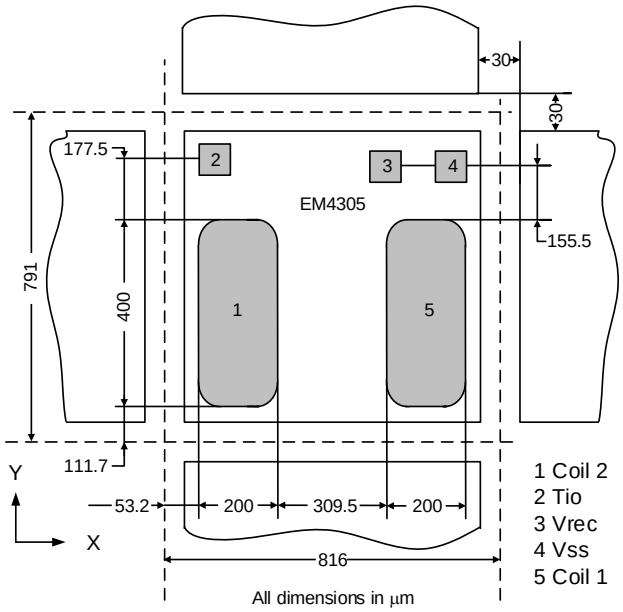


Figure 16

EM4305 Pad Location (V7 and V8)



EM Standard bump size 102µm x 102µm
Big bump size 200µm x 400µm
Scribe line width 30µm

Figure 17

Pad Description

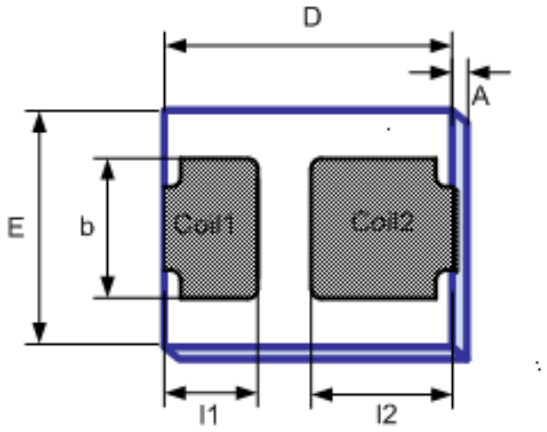
Pad	Name	Function
1	Coil 2	Coil connection 2
2	Test	Test purpose (NC) - Active pad
3	V test 1	Test purpose (NC) - Active pad
4	V test 2	Test purpose (NC) - Active pad
5	Coil 1	Coil connection 1

Table 13

Note: Test pads (Test, Vtest1 and Vtest2) are electrically active and used for test purposes only, no connection allowed.

Packaging information

2 leads Plastic Package: EMDFN02



Package mechanical dimensions:

	A	D	E	B	l1	l2
Size	0.76	2.20	1.78	1.07	0.71	1.08
Tolerance	0.10	0. 15	0.15	0.05	0.05	0.05

Table 14

Note: all dimensions in mm.

Package material	RoHS compliant
Size	2.2 x 1.78 mm [86.6 x 70 mils]
Thickness	0.76 mm [30 mils]

Table 15

Packing method

3 types of packing method are available:

- ❑ Loose form (Aluminum canisters)

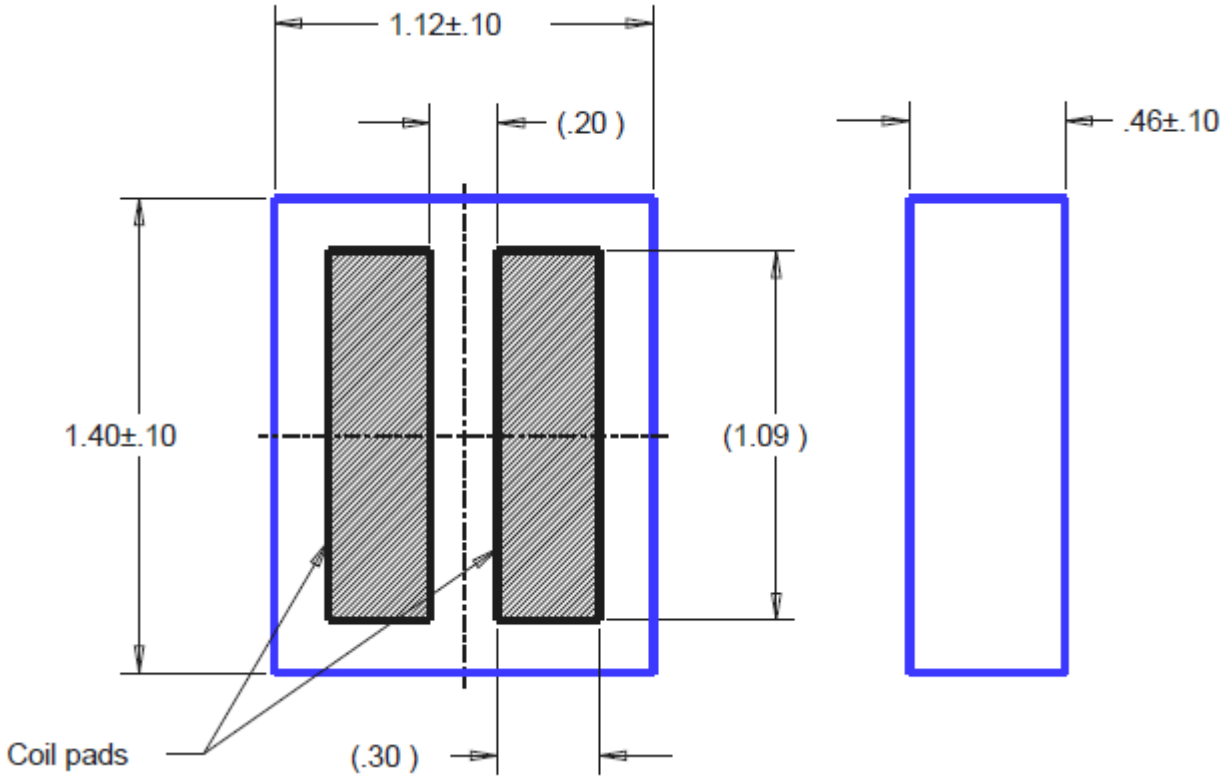
Ordering Information – Package IC

Part Number	IC Reference	IC Resonant capacitor	Delivery format	Remarks
EM4205V4DF2C+	EM4205	210pF	Loose form	Resonant capacitor trimmed (tolerance +/- 3%)
EM4305V3DF2C+	EM4305	330pF	Loose form	

Table 16

2 leads Plastic extremely thin small outline package; body 1.1 x 1.4 x 0.46 mm: EMDFN403

Package mechanical dimensions:
All dimensions in inches [mm].



Packing method
2 types of packing method are available:
- ❑ Loose form (Aluminum canisters)

Ordering Information – Package IC

Part Number	IC Reference	IC Resonant capacitor	Delivery format	Remarks
EM4305V7DF403C+	EM4305	250pF	Loose form	
EM4305V8DF403C+	EM4305	330pF	Loose form	

Table 17

Ordering Information – Die form

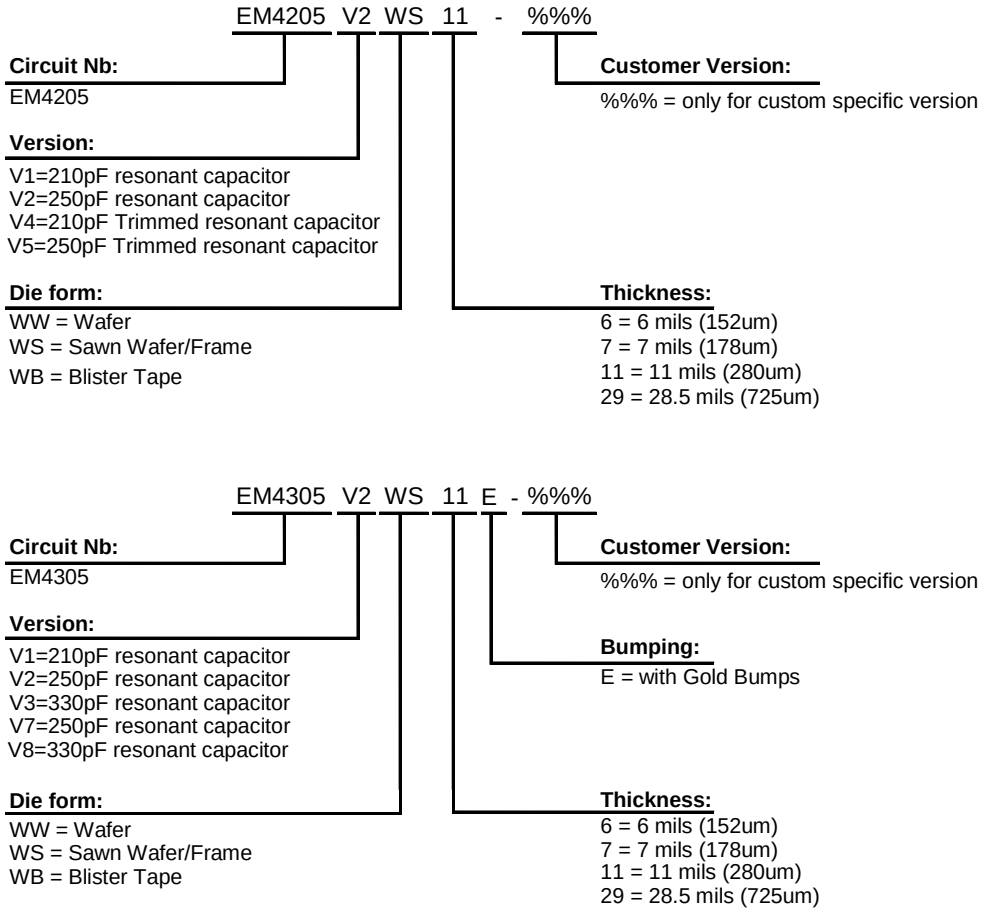


Figure 17

Remarks:
EM4205: for a sawn or un-sawn wafer delivery, the failed die identification is covered by ink dots applied to the wafer.
EM4305: for a sawn or un-sawn wafer delivery, the failed die identification is covered by electronic wafer mapping. No ink dots are applied to the wafer.
For specifications of delivery form, including gold bumps, Blister, as well as possible other delivery form or packages, please contact EM Microelectronic-Marin S.A.

Standard Versions & Samples:
The versions below are considered standards and should be readily available. For other versions or other delivery form, please contact EM Microelectronic-Marin S.A.

Part Number	Package	Delivery Form
EM4205V2WS11	sawn wafer	Wafer on frame
EM4305V1WS11E	sawn wafer	Wafer on frame
EM4305V2WS11E	sawn wafer	Wafer on frame
EM4305V3WS11E	sawn wafer	Wafer on frame
EM4305V7WS11E	sawn wafer	Wafer on frame
EM4305V8WS11E	sawn wafer	Wafer on frame
EM4305VXYYY-%%%	Custom	Custom

Table 18